WHAT IS CLAIMED IS:

    1.   A communications system comprising:
5   a decision feedback equalizer adapted to reduce channel related distortion in received data, wherein the decision feedback equalizer generates equalized data; and
        a clock and data recovery circuit coupled to the equalizer, wherein the clock and data recovery circuit 10 generates an extracted clock signal having an adjustable phase offset from the equalized data to compensate for processing delays in the decision feedback equalizer and wherein the decision feedback equalizer includes a retimer that generates recovered equalized data from the equalized data in response 15 to the extracted clock signal.

    2.   The communications system of claim 1 wherein the decision feedback equalizer comprises a summer that generates a combined signal by combining an equalized feedback signal 20 with the received data to reduce the channel related distortion.

    3.   The communications system of claim 2 wherein the decision feedback equalizer further comprises a slicer coupled 25 to the summer, wherein the slicer generates the equalized data by converting the combined signal to a binary signal and wherein the clock and data recovery circuit generates the extracted clock signal having an adjustable phase offset from the binary signal.
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    4.   The communications system of claim 3 wherein the equalizer retimer comprises a flip flop coupled to the slicer and the clock and data recovery circuit and wherein the flip flop generates recovered equalized data from the binary signal 35 in response to the extracted clock signal.

5.   The communications system of claim 1 wherein the clock and data recovery circuit comprises:

a phase detector for generating a phase error signal in accordance with difference in phase of the extracted clock signal and the equalized data;

a voltage controlled oscillator for generating the extracted clock signal as a function of the phase error signal; and

a delay coupled between the voltage control oscillator and the phase detector for adjusting phase of the extracted clock signal.

6.   The communications system of claim 1 wherein the clock and data recovery circuit comprises:

a phase detector for generating a phase error signal in accordance with difference in phase of the extracted clock signal and the equalized data; and

a voltage controlled oscillator for generating the extracted clock signal as a function of the phase error signal, wherein the phase detector adjusts the phase error signal in response to a phase offset signal to adjust phase of the extracted clock signal.

7.   A communication system comprising:

a transmitter transmitting an information signal over a communication media; and

a receiver coupled to the communication media for receiving the transmitted information signal, wherein the receiver comprises:

a decision feedback equalizer adapted to reduce channel related distortion in received data, wherein the decision feedback equalizer generates equalized data, and

a clock and data recovery circuit coupled to the equalizer, wherein the clock and data recovery circuit generates an extracted clock signal having an adjustable phase offset from the equalized data to compensate for processing delays in the decision feedback equalizer and wherein the decision feedback equalizer includes a retimer that generates recovered equalized data from the equalized data in response to the extracted clock signal.

8.   The communications system of claim 7 wherein the decision feedback equalizer comprises a summer that generates a combined signal by combining an equalized feedback signal with the received data to reduce the channel related distortion.

9.   The communications system of claim 8 wherein the decision feedback equalizer further comprises a slicer coupled to the summer, wherein the slicer generates the equalized data by converting the combined signal to a binary signal and wherein the clock and data recovery circuit generate the extracted clock signal from the binary signal.

10. The communications system of claim 9 wherein the equalizer retimer comprises a flip flop coupled to the slicer and the clock and data recovery circuit and wherein the flip flop generates recovered equalized data from the binary signal data in response to the extracted clock signal.

11. The communications system of claim 10 wherein the equalizer further comprises a multiplier coupled to the retimer and wherein the equalizer applies an equalization coefficient to the recovered equalized data to generate the equalized feedback signal.

12.   A communications system comprising:

a decision feedback equalizer adapted to reduce channel related distortion in received data, the decision feedback equalizer comprising:

a summer that combines an equalized feedback signal with the received data,

a slicer coupled to the summer, wherein the slicer converts the combined signal to a binary signal;

a retimer coupled to the slicer, wherein the retimer generates recovered equalized data from the binary signal in response to an extracted clock signal, and

a multiplier coupled to the retimer, wherein the multiplier applies an equalization coefficient to the recovered equalized data to generate the equalized feedback signal; and

a clock and data recovery circuit coupled to the slicer, wherein the clock and data recovery circuit generates the extracted clock signal from the binary signal, and wherein the clock and data recovery circuit adjusts phase of the extracted clock signal to compensate for processing delays in the decision feedback equalizer.

13.   The communications system of claim 12 wherein the clock and data recovery circuit comprises:

a phase detector for generating a phase error signal in accordance with difference in phase of the extracted clock signal and the binary signal;

a voltage controlled oscillator for generating the extracted clock signal as a function of the phase error signal; and

a delay coupled between the voltage control oscillator and the phase detector for adjusting phase of the extracted

clock signal.

5   14. The communications system of claim 12 wherein the
clock and data recovery circuit comprises:
        a phase detector for generating a phase error signal in
accordance with difference in phase of the extracted clock
signal and the binary signal; and
10   a voltage controlled oscillator for generating the
extracted clock signal as a function of the phase error
signal, wherein the phase detector adjusts the phase error
signal in response to a phase offset signal to adjust phase of
the extracted clock signal.
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        15. A communications system comprising:
        a decision feedback equalizer adapted to reduce channel
related distortion in received data, wherein the decision
feedback equalizer generates equalized data; and
20   a clock and data recovery circuit coupled to the
equalizer, wherein the clock and data recovery circuit
generates an extracted clock signal from the equalized data,
and wherein the decision feedback equalizer includes a retimer
that generates recovered equalized data from the equalized
25   data in response to the extracted clock signal; and
        a real time optimizer coupled to the clock and data
recovery circuit, wherein the real time optimizer generates a
phase adjust signal and wherein the clock and data recovery
circuit adjusts phase of the extracted clock signal in
30   response to the phase adjust signal to compensate for
processing delays in the decision feedback equalizer.

        16. The communications system of claim 15 wherein the
decision feedback equalizer comprises a summer that combines
35   an equalized feedback signal with the received data to

generate the equalized data.

5   17. The communications system of claim 16 further comprising a monitor circuit for generating a sum square error signal from the equalized data and wherein the real time optimizer adjusts the phase adjust signal to reduce the sum square error signal.

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         18. The communications system of claim 17 wherein the decision feedback equalizer further comprises a slicer coupled to the summer, wherein the slicer converts the combined signal to a binary signal and wherein the clock and data recovery

15   circuit generates the extracted clock signal having an adjustable phase offset from the binary signal.

         19. The communications system of claim 18 wherein the equalizer retimer comprises a flip flop coupled to the slicer

20   and the clock and data recovery circuit and wherein the flip flop generates the recovered equalized data from the binary signal in response to the extracted clock signal.

         20. The communications system of claim 15 wherein the

25   clock and data recovery circuit comprises:
         a phase detector for generating a phase error signal in accordance with difference in phase of the extracted clock signal and the equalized data;
         a voltage controlled oscillator for generating the

30   extracted clock signal as a function of the phase error signal; and
         a delay coupled between the voltage control oscillator and the phase detector for adjusting phase of the extracted clock signal.

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21.   The communications system of claim 15 wherein the clock and data recovery circuit comprises:

a phase detector for generating a phase error signal in accordance with difference in phase of the extracted clock signal and the equalized data; and

a voltage controlled oscillator for generating the extracted clock signal as a function of the phase error signal, wherein the phase detector adjusts the phase error signal in response to a phase offset signal to adjust phase of the extracted clock signal.

22.   A method of reducing channel related distortion in received data comprising:

providing received data to a decision feedback equalizer;

generating, by the decision feedback equalizer, a binary signal according to the received data;

generating a phase delay signal;

extracting a clock signal from the binary signal according to the phase delay signal; and

retiming the binary signal according to the clock signal.

23.   The method of claim 22 wherein a real time optimizer generates the phase delay signal.

24.   The method of claim 22 wherein generating the phase delay signal comprises delaying a signal from a voltage control oscillator to a phase detector.

25.   The method of claim 22 wherein generating the phase delay signal comprises generating a distortion error signal in accordance with a soft decision signal generated by the decision feedback equalizer.

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     26. The method of claim 25 wherein a real time optimizer generates the phase delay signal by processing the distortion
5   error signal.

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